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Review of On-Chip Network Topology for Clos Permutation Network

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Abstract: **The clos networks are the class of multistage switching network topologies that provide alternate paths between inputs and outputs. It is one of the known connection networks in processing system and distributed Systems, which are extensively used in many fields such as telecommunication networks, ATM switches and data transmission. One of the key challenges in designing a clos network switch for a high speed environment is designing the architecture switch module and arbitration algorithms so as to provide wide range of traffic patterns and resolve contention between the stages of the switches in clos network. So efficient various routing algorithms and different techniques are proposed to solve problem which occur in clos network and also to achieve guaranteed throughput, latency, bandwidth, power and area parameters. In this paper, different techniques and routing algorithms for a clos permutation network are reviewed.**

Keywords: **Multistage interconnection networks (MINs), clos Network , parallel routing, rearrangeable, non-blocking, Blocking, permutation network, Clos network on chip (CNOC), Buffer less clos network (BLOCON), Network-on-chip (NOC).**

I. INTRODUCTION

The network on chip is an emerging for communications within large VLSI systems implemented on a single silicon chip. As the number of IP modules in system-on-chip increases bus-based interconnection architectures may prevent these systems to meet performance required by many applications like parallel processing, scientific computing, speech signal processing, Image and video signal processing and Information technologies. For systems with demanding parallel communication requirements buses may not provide the required bandwidth, latency and power consumption and also buses are an increasing inefficient way to communicate since only one source can drive the bus at a time, thus limiting bandwidth. So a solution for such a communication bottleneck is the use of an embedded switching network called network- on-chip. There are different network topologies like Star, Ring, Clos, etc., which are used for communication but this paper mainly concentrates on three stage clos network.

II. BRIEFLY REVIEWS OF CLOS NETWORK

In 1953,C. Clos published the first fundamental study [19] of non-blocking connection networks. on-blocking networks have applications in communications like telephone switching networks and Communication networks among processors or between processors and memory devices [20].

A switching network is strictly non-blocking if these always exists a Connection path from any idle input to any idle output in the presence of existing connections, regardless of how the existing connection paths were selected[21] non-blocking and rearrangeable MINs provide multipath between every I/O pair (eg., processor to processor or processor to memory) and can realize all I/O permutations at the same time. Non blocking switching networks have been favored in switching systems because they can be used to setup any conflict free ,one-to-one I/O connection paths. This type of network include hypercube, cube-cube-connected-cycles, butterfly networks, omega network flip networks, de bruijin graphs, shuffle exchange networks, banyan networks, delta network, bi delta networks ,k-ary butterflies and Benes networks .

Clos networks are well-know universal multistage networks that realize all permutations and network is capable of connecting its outputs according to any N! permutations. A permutation network (also known as a rearrangeable network) is a system in which some number of terminals called inputs, an equal number of other terminals called outputs and some numbers of switches are interconnected by means of wires. A way to realize a permutations operation in a parallel or distributed computing system is to use a multistage interconnection network. A MINs usually consists of multiple stage of 2x2 switches with adjacent stages connected by mapping function .

Clos networks are important class of switching network due to their modular structure and much lower cost compared with crossbar [21]. Clos network were first defined by clos in the 1950 [22] .According to [22] clos networks can be any three stage with m'<m is blocking ; any three stage clos network with m'>-n is rearrangeable; any three stage clos network m'>-2m-1 is strict-sense non-blocking. Where N/m switches of size mxm' are used at input stage I and m' switches of size N/m xN/m are used at intermediate stage II.

I. Clos Network:

Clos network is a multistage network topology is a multistage network topology which is used in switching technique for data transfer in three stages, and also it has sixteen inputs and outputs , each path is select dynamically according to the input given. The main advantage of network is that connection between a large number of input and output ports can be made by using only small-sized switches In figure 4, n represent the number of sources which feed into each of the m ingress stage crossbar switches. There is exactly one connection between each ingress stage

switch and each middle stage switch. And each middle stage switch is connected exactly once to each egress stage switch. Clos network is non-blocking when m>n-1, ingress/egress stage has r n x m switches, middle stage has m r x r switches, and each switch at ingress/egress stage connects to all m middle switches. This network has a rearrangeable property that can realize all possible permutations between its input and outputs. The variety of the three stage clos network with a modest number of middle–stage switches is to minimize implementation cost, whereas it still has a rearrange able property for the network.

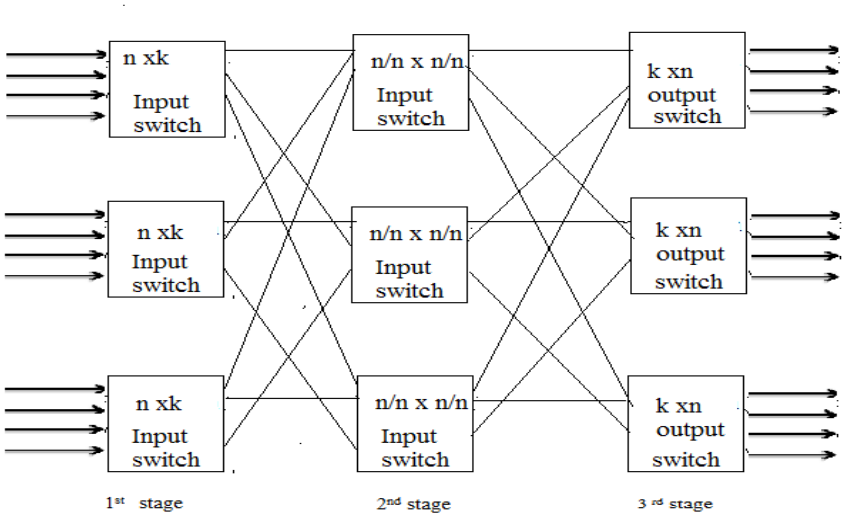

Fig 1: shows the 3-stage clos network

III. LITERATURE SURVEY

Soung C. Liew et.al. in their paper [1] investigates in detail the blocking and non-blocking behavior of Multirate clos switching network at connection/virtual connection level. The result are applicable to Multirate circuit and fast-packet switching systems. Necessary and sufficient non-blocking conditions are derived analytically. Based on the result, on optimal bandwidth partitioning scheme is proposed to reduce switch complexity while maintaining the non-blocking property. The author proposed a novel simulation model that filters out external blocking events without distorting the bandwidth and fan-out distributions of connection request and also the authors shows the point-to-multipoint connections and results indicate that situations with many large-fan-out connection request do not necessarily require a switch architecture of higher complexity compared to that with only point-to-point request.

Eiji oki et.al in their paper[2] describes the two round-robin based dispatching schemes to overcome the throughput limitation of the random dispatching scheme. First, they introduce a concurrent round-robin dispatching scheme for the clos network switch . the concurrent round-robin scheme provides high throughput without expanding internal bandwidth .and also implementation of concurrent round-robin dispatching is very simple because only simple round-robin arbiter are adopted. And the results shows that concurrent round-robin dispatching scheme achieves 100% throughput under uniform traffic and offered a load reaches 1.0, the pointers of round robin arbiters at first and second stage modules are completely desynchronized and contention is avoided. second, they introduce a concurrent master-slave round-robin dispatching scheme as an improved version of concurrent round-robin dispatching to make it more scalable. And results shows that concurrent master slave dispatching preserves the advantages of concurrent round-robin dispatching ,and its reduces the scheduling time by 30% or more when arbitration time is significant and has a dramatically reduced number of cross points of the interconnection wires between round-robin arbiters in the dispatching scheduler with a ratio of 1,where is the switch size. this makes the concurrent master slave dispatching easier to implementation than concurrent round-robin dispatching when the switch size becomes large.

Jonathan S. Turner [3] in this paper describes how clos results have been generalized to systems that support connections with varying bandwidth requirements these generalizations have extended the application of clos networks well beyond their original technological context and have led to number of interesting new results, especially in connection with systems that support multicast communication.

Yu-Hsiang Kao et.al [4] in their paper describes that a high radix router architecture with virtual output queue buffer structure and packet mode dual round robin matching scheduling algorithm to achieve high speed and high throughput in CNOC. A heuristic floor planning algorithm to minimize the consumption caused by the long wires. Experimental result shows that the throughput of 64 nodes 3-stage CNOC under uniform traffic increase from 62% to 78% by replacing the baseline routers with PDRM VOQ routers. And also author compared CNOC with other NOC topologies and found that using the new design techniques, CNOC has the highest throughput, lowest zero-load latency, and best power efficiency.

Feng Wang [5] in their paper describes that the author consider using the clos network to scale high performance routers, especially the space –memory-space packet switches. In circuit switching, the clos network is responsible for pure connections and internal links are the only blocking sources. In packet switching, however, the buffer cause additional blockings. So the author suggest a method a scalable packet switch architecture that is call the central stage buffered clos network .then and author analyze the memory requirements for the central stage buffered clos networks to be strictly non-blocking, especially for emulating an output queuing packet switch. And results Show that even with the additional memory blocking the central stage buffered clos network still inherits advantages from the clos network.eg., modular design and cost efficiency.

Tony T.Lee et.al. developed a new parallel routing algorithm in 1996[6], by solving a set of Boolean equations which are derived from the connection request and the symmetric structure of the Benes network. The time complexity of algorithm is O(N),where N is the network size of Benes network. This algorithm described in [8] can be extended and applied in clos network if the number of Central modules is M= where m is positive integer and the time complexity is O(log N X log M).

In 2006, S.Q. Zhen et al.in [7] presented an efficient parallel an efficient parallel algorithm coloring for routing clos networks, and a hardware implementation Hard coloring of distributed pipeline routing algorithm. According to authors the best know sequential algorithm for rearrangeable clos network has time complexity O(N logN) and best know parallel routing algorithm for rearrangeable N X N clos network C (n,m,r) has time complexity O (N), when m is a power of 2. Author ‘s parallel routing algorithm takes O (N) time for optimized non-blocking C(n,m,r) Networks.

Ajay Joshi et al.in [8] in their paper the author consider a silicon photonics is a promising new interconnect technology which offers lower power, higher bandwidth density and shorter latencies than electrical interconnects. And author explore using photonics to implement low-diameter non-blocking crossbar and clos network. And author analytical modeling show that a 64-tile photonic clos network consumes significantly less optical power, thermal tuning, power, and area compared to global photonic crossbars over a range of photonic device parameters. Compared to various electrical on-chip networks, and also the simulation results indicate that a photonic clos network can provide more uniform latency and throughput across a range of traffic patterns while consuming less power.

For the phonic NOC architectures, Kao et al[9] proposed a buffer less approach, named the buffer less clos network.(BLOCON).The BLOCON does not uses the VC buffers and could thus reduce the power consumption and

latency. The BLOCON has been compared to the buffered photonic Clos network (BPCN), flattened butterfly (Fbfly), 2D mesh, and CMESHx2 networks respectively. The result have indicated that the increases in the throughput for the BLOCON was about 128%,116%,43%,and 38%, as compared to the 2Dmesh, CMESHx2,Fbfly,and BPCN, Respectively. The BLOCON had also consumed 62%,61%,60% and 40%, lesser energy, as compared to the2Dmesh,CMESHx2, Fbfly,and BPCN ,respectively.

Srinivasan murali et.al. [10] in their paper describes a method for reducing the hardware complexity of the NOC by automatically configuring the architecture of the NOC switches to suit the application traffic characteristics. The crossbar matrix and arbiters of each switch in the NOC design are customized to support the traffic flows utilizing that switch. This application specific switch customization is integrated with existing design Flow, which automates Noc topology synthesis, mapping, RTL codes and physical layout generation. And author shows the results the proposed switch customization techniques leads to large reduction in the NOC switch area (28% on average) and power consumption (21% on average) .Moreover , the critical paths of switches reduces significantly, thereby leading to significant speed-up of the NOC design.

David M. Koppelman et al.in [11] in their paper describes that a lower bound on the amount of information necessary to compute the switch settings for a three-stage clos network is derived. The bound is derived by considering the effect of the a family of permutations, called balanced multi hops, on the settings of the switches of clos network. And carefully selecting these permutations, it is proven that there exist at least one switch in each stage whose setting depends upon at (k-3)(m/2+1)/2 assignments in permutations to be routed for k >4 where m is the number of central stage switches and K is the number of input and output stage switches. Lower bounds on the routing time of a three-stage clos network on a variety of machine models follow immediately from these results. In particular any constant fan-in implementation of any routing algorithm For such a network should have a time lower bound of n(logmk).

Xiaowen Wu et.al [12] in their paper describes that the network is composed of an inter-chip sub network and multiple intra-chip sub networks closely coordinate with each other to balance the traffic. The author proposed network effectively explores the distinctive properties of optical signals and photonic devices, and Dynamically partitions each data channel into multiple Sections and author results shows the network can achieve higher throughput with lower power consumption than alternative designs under most of synthetic traffics and real applications.

Roberto Rojas-cessa et.al [13] in their paper Describes that the author use the packet switching , the three clos network architecture uses small switches as modules to assemble a switch with large number of ports or aggregated ports with high data rates. However, the configuration complexity of packet clos Network switches is high as port matching and path routing must be performed. In the majority of the existing schemes, the configuration process performs routing after port-matching is achieved. And author proposed matching scheme, and shows that the numberof a clos network switch can be reduced to two, and the author call this the two-stage clos network packet switch.

Xin Yuan [14] in their paper describes that the Concept of non-blocking interconnects, which is often used by system vendors, has only been studied in the telephone communication environment with the assumption of a centralized controller. Such non-blocking networks do not support non-blocking communications in computer communication environments where the network control is distributed the author investigate folded clos network that are non-blocking in computer application environments and establish non blocking conditions for various routing scheme including deterministic routing and adaptive routing .

Pimental et.al [15] In their paper describes that author shows the simulation study is presented in Order to evaluate worm hole routed mesh of clos communication networks. It is shown that this type of network can substantially reduce contention as compared to flat mesh networks. furthermore, the author found that increasing the number of flit buffers on router devices does not necessarily lead to improved communication performance. For some application loads it may even result in a loss of performance.

Yuanynan et .al [16] In their paper describes that the author analyze the fault tolerance capability of the three stage rearrangeable clos network. And established a fault model on losing contact faults in theSwitches of the network. And author suggested a method necessary and sufficient condition on the losing contact faults a clos network can tolerate for any given permutation .and also develop an efficient fault tolerant algorithm for a rearrangeable clos network based on these results.

Steve Scott et.al [17] In their paper describes that The radix 64 folded clos network of the Cray black Widow scalable vector multiprocessor and this will implemented by using high –radix router with many narrow channels are able to take advantage of the higher pin density and faster signaling rates available in modern ASIC technology .

Moo-Kyung kang et.al [18] in their paper describes that the proposed a competition free memory-memory-memory (CFM3) switch which is a three stage clos network switch with buffered center. The CFM3 is a free from reordering problem due to simple control mechanism .and the results shows the delay of the proposed CFM3 achieves 100% throughput under uniformly distributed four class traffic with strict priority policy while traditional MSM switch records about 77% throughput.

IV. CONCULSION

In this paper, presented a review of number of different techniques to design a three stage clos network and also number of routing algorithm to achieve a better throughput, bandwidth ,latency, are reviewed. It also describes number techniques of blocking and non-blocking networks to achieve better performance and also this provides a basis for the further investigation and application of these ideas to other topologies, and open new dimensions for improving these techniques to obtain newer better designs.

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REFERENCES

[1] Soung C.Liew,Ming-Hung Ng, and Cathy W. Chan, “Blocking and non -blocking Multirate clos switching networks,’’ IEEE/ACM Trans.on networking , vol.6, no.3, June 1998,pp.307-318.

[2] Eiji oki, Zhigang Jing ,Roberto Rajos-cessa, and H.Jonathan choa.”Concurrent round robin based dispatching schemes for clos network switches “,IEEE / ATM Trans on networking,vol.10,no.6 ,December 2002.pp.830-844.

[3] JonathanS. Turner and Riccardo Melen,“Multirate Clos networks”, IEEE communication Magazine. October 2003,pp1-11.

[4] Yu-Hsiang Kao, Najila Alfaraj,Minag Yang. And H.Jonathan Chao, Design of “High–Radix clos network –on-chip”. IEEE international symposium on Network-on-chip ,2010, pp.181-188.

[5] Feng Wang and Mounir Handhi,“Strictly non-blocking conditions for central-stage buffered clos-network”, IEEE communicstions,vol.12,no.3, march 2008,pp.206-208.

[6] Tony T.Lee and Soung-Yne Liew, “Parallel routing algorithms in benes-clos network”, IEEE, 1996, pp.279-286.

[7] S.Q. Zheng, Ashwin Gumaste and Enyne Lu, “A practical fast parallel routing architecture for clos networks”. ANCS’ 06, San Jose, California USA , pp.21-30, December 3-5, 2006.

[8] Ajay Joshi, Christopher Batten ,Yong-Jin kwon ,Scott Beamer,Imran Shamim, Silicon-Photonic clos networks for global on-chip communication” International Symposium on networks-on-chip, may 2009.

[9] Kao.Y ,Chao H. “ Design of a buffer less Photonic clos network-on-chip architecture, IEEE Trans comut. Vo1.99, 2012.

[10] SrinivasanMurali, SalvatoreCarta, Marsino Camplani“Routing aware hardware customization for networks–on-chips”,IEEE Trans.2006.

[11] David M. Koppelman and A.Yavuz Orug , “The complexity of routing in clos permutation networks”, IEEE Trans. on information theory, vol.40,n0.1, January 1994,pp.278-284.

[12] Xiaowen wu, Jiang xu,Yaoyaoye,Xuan Wang, et.al An Inter/Intra-chip optical network for many core processors”. IEEE Trans.on Very Scale Integration syst 2014. Pp.1-14.

[13] Roberto Rajos-cessa.and chuan-Bi Lin, "Scalable two stage clos network switch and module-first matching", IEEE Trans.June 2006

[14] Xin Yuan "On non-blocking folded clos networks in compute communication environments"

[15] .A.D.Pimental and L.O. Hertz berger " Simulation Of a mesh of clos wormhole network.

[16] Y.yang and J.wang, A fault-tolerant rearrangeable permutation network", IEEE Trans.Comput., Vol.53,no.4,pp.141-246,April.2004.

[17] Steve Scott,Dennis Abts,Johan kim ,and Wiliam J.Dally "The black widow high radix clos network.

[18] Moo-Kyung Kang and Chong-Min kyung , "Three stage clos network switch architecture with buffered center stage for multi-class traffic". Journal circuit system. December 2005.

[19] V.Benes ,Mathematical theory of connecting networks and telephone traffic,vol.17,new york ,academic ,1965.

[20] Sergio A. Felperin ,Luis Gravano,et.al Routing techinques for massive parallel communication", Proceedings of the IEEE, Vol.79,no.4,pp.488-503,April 1991.

[21] S.Q.Zheng, Ashwin Gumaste and Enyne Lu," A practical fast parallel routing architecture for clos networks " ANCS' 06,San Jose California USA, pp.21-30,December 3-5-2006

[22] Marcello Coppola, M iltos D, Grammataikis Riccardo Locatelli,Giuseppe Maruccia and Lorenzo Pieralisi, "Design of cost–efficent interconnect processing units" CRC press Taylor and Grancis Group.

[23] Enyue Lu, and S.Q. Zheng, " Parallel routing algorithms for non-blocking electronic and photonic switching networks", IEEETrans.on parallel and distributed systems,vol.16, no.8, pp.702-713, August 2005.